ADC/DAC/Analog interface
Analog I/O

- Analog inputs – convert to digital using an Analog to Digital converter (A/D or ADC)
- Analog output – convert digital output to analog using a Digital to Analog converter (D/A or DAC)
- A/D outputs and D/A inputs can be attached to digital I/O ports
- Design issues to consider – number of bits of accuracy, conversion time delay, and sample rate needed by application
The MCP3008 10-bit 200Ksps A/D chip used in Phidget modules has an SPI interface.
Off-the-shelf ADC

- Resolution – smallest distinguishable change in input
- Precision – number of distinguishable inputs
- Accuracy – the absolute error of the entire system
- Monotonic – no missing codes
- Linear – constant resolution
- Speed – time to convert
Analog-digital interface
Processing analog signal

Signal Processing
- Measurand
- Sensor
- Conditioner
- Analog Processor
- LPF
- ADC

Analog Processing

Digital Processing
- DSP
- DAC
- Analog Processor
- LPF
Analog input signal
Analog input signal

• For periodic waveforms, the duration of the waveform before it repeats is called the period of the waveform.

• The rate at which a regular vibration pattern repeats itself (frequency = 1/period).
Frequency of a Waveform

• The unit for frequency is cycles/second, also called Hertz (Hz).

• The frequency of a waveform is equal to the reciprocal of the period.

\[ \text{frequency} = \frac{1}{\text{period}} \]
Frequency of a Waveform

• Examples:
  
  frequency = 10 Hz  
  period = .1 (1/10) seconds

  frequency = 100 Hz  
  period = .01 (1/100) seconds

  frequency = 261.6 Hz (middle C)  
  period = .0038226 (1/ 261.6) seconds
Waveform Sampling (Quantization)

- To represent waveforms on digital computers, we need to digitize or sample the waveform.

- side effects of digitization:
  - introduces some noise
  - limits the maximum upper frequency range
Sampling rate

- The sampling rate (SR) is the rate at which amplitude values are digitized from the original waveform.
  - CD sampling rate (high-quality): \( SR = 44,100 \) samples/second
  - medium-quality sampling rate: \( SR = 22,050 \) samples/second
  - phone sampling rate (low-quality): \( SR = 8,192 \) samples/second
Sampling rate

• Higher sampling rates allow the waveform to be more accurately represented
Nyquist Theorem

- **Nyquist Theorem:**
  We can digitally represent only frequencies up to half the sampling rate.

  - **Example:**
    CD: $SR = 44,100 \text{ Hz}$
    Nyquist Frequency $= \frac{SR}{2} = 22,050 \text{ Hz}$

  - **Example:**
    $SR = 22,050 \text{ Hz}$
    Nyquist Frequency $= \frac{SR}{2} = 11,025 \text{ Hz}$
Nyquist Theorem

Sampling rate (SR) > 2 \( f_{\text{max}} \)

\( f_{\text{max}} \) is the largest signal frequency of interest
Nyquist Theorem and Aliasing

• **Graphical Example 1a:**
  - $SR = 20,000 \text{ Hz}$
  - Nyquist Frequency $= 10,000 \text{ Hz}$
  - $f = 2,500 \text{ Hz}$ (no aliasing)
Nyquist Theorem and Aliasing

- **Graphical Example 1b:**
  - SR = 20,000 Hz
  - Nyquist Frequency = 10,000 Hz
  - f = 5,000 Hz (no aliasing)
Nyquist Theorem and Aliasing

• **Graphical Example 2:**
  - SR = 20,000 Hz
  - Nyquist Frequency = 10,000 Hz
  - f = 10,000 Hz (no aliasing)
Nyquist Theorem and Aliasing

• **Graphical Example 2:**
  – BUT, if sample points fall on zero-crossings the sound is completely cancelled out
Nyquist Theorem and Aliasing

• **Graphical Example 3:**
  – SR = 20,000 Hz
  – Nyquist Frequency = 10,000 Hz
  – f = 12,500 Hz, f' = 7,500
Nyquist Theorem and Aliasing

• **Graphical Example 3:**
  – Fitting the simplest sine wave to the sampled points gives an aliased waveform (dotted line below):
Sample of sine wave at different freq.

- **a. Analog frequency = 0.0 (i.e., DC)**
- **b. Analog frequency = 0.09 of sampling rate**
- **c. Analog frequency = 0.31 of sampling rate**
- **d. Analog frequency = 0.95 of sampling rate**
Processing analog signal
Low pass filter

- Allow only low frequency value to pass
- Prevent aliasing
Layout of ADC

ADC

Sampler → Quantizer → Coder

x(t) → x_U(t) → x_q(t) → b bits

p(t)
ADC precision

• Number of ADC bit output (n):
  \[ n = \frac{\text{input range (r)}}{\text{input resolution} \Delta y} \]

  E.g., input range of 1, and resolution of 0.0001

  \[ n = 10000 \text{ alternatives or 15 bits value} \]

Assume linear ADC
Sample and hold circuit
Sample and hold circuit

- Using op-amp to hold signal strength
- Unity gain buffer
Sample and hold signal
Hold circuit output

b. Sampled analog signal
Quantized output

c. Digitized signal
## Convert analog value to digital value

<table>
<thead>
<tr>
<th>Bipolar codes</th>
<th>Offset binary</th>
<th>2s binary</th>
</tr>
</thead>
<tbody>
<tr>
<td>+5.00</td>
<td>1111</td>
<td>0111</td>
</tr>
<tr>
<td>+2.50</td>
<td>1100</td>
<td>0100</td>
</tr>
<tr>
<td>+0.04</td>
<td>1000</td>
<td>0000</td>
</tr>
<tr>
<td>+0.00</td>
<td>1000</td>
<td>0000</td>
</tr>
<tr>
<td>-2.50</td>
<td>0100</td>
<td>1100</td>
</tr>
<tr>
<td>-5.00</td>
<td>0000</td>
<td>1000</td>
</tr>
</tbody>
</table>
ADC types

- Flash ADC
  - fast
- Successive Approximation ADC
  - most popular
- Sigma Delta ADC
  - highest output precision
Flash ADC

• Use reference voltage and differential op-amp to generate digital output
• Fast conversion
• To increase the number of bits, it requires larger hardware support
Two-bit flash ADC

Vin | X3 | X2 | X1 | Z1 | Z0
---|----|----|----|----|----
V<2.5 | 0  | 0  | 0  | 0  | 0  
2.5≤V<5.0 | 0  | 0  | 1  | 0  | 1  
5.0≤V<7.5 | 0  | 1  | 1  | 1  | 0  
V≥7.5 | 1  | 1  | 1  | 1  | 1  

Diagram of the two-bit flash ADC circuit.
Flash converter

Fig. 18.12 Flash Converter
256R ladder network
Successive Approximation ADC

• Similar to Flash ADC, but use only one set of hardware
• Require longer time
• Fixed size of hardware
• Widely used
Successive Approximation ADC

Vin

5V

Digital output

N bit ADC

Clock

n

N bit Successive Approximation

Done

Go
The MCP3008 10-bit 200Ksps A/D chip used in Phidget modules has an SPI interface.
Successive approximation counting
Block diagram of internal AD converter

† Multiplexed with port inputs
AD converter
3-bit AD converter

![Diagram of 3-bit AD converter with various error considerations including ideal curve, zero error, full-scale error, and nonlinearity.](image-url)
Delta-Sigma ADC

- Quantization noise is uniformly distributed among frequency spectrum
- Using over-sampling technique to reduce the impact of quantization noise
- Results in higher bit-precision
- Slow
Frequency domain

SNR = 6.02N + 1.76dB for an N-bit ADC
Oversampling by K times
Delta-Sigma circuit

Fig. 1 - Block Diagram Delta Sigma ADC

1 = 0.2V INPUT

1V IMPULSE

0V

SUM 0.2V

- 0.2V

0V THRESHOLD

4

INTEGRAL

TRIGGER

1 = 0.4V INPUT

1V IMPULSE

0V

0.4V SUM

- 0.6V

0V THRESHOLD

4

INTEGRAL

TRIGGER
Signal pin of AD converter
Digital to Analog Converter (DAC)
Layout of DAC

![Diagram of DAC layout](image-url)
Analog of digital conversion

![Graph showing an impulse train with labeled axes for time and amplitude.](image-url)
Analog voltage of zero order
Reconstruction
Summing Amplifier

Since $i_- = 0$, $i_3 = i_1 + i_2$,

$$v_o = -\frac{R_3}{R_1}v_1 - \frac{R_3}{R_2}v_2$$

- Scale factors for the 2 inputs can be independently adjusted by proper choice of $R_2$ and $R_1$.
- Any number of inputs can be connected to summing junction through extra resistors.
- This is an example of a simple digital-to-analog converter.
Binary weight register method

\[ V_0 = -R_f \left( \frac{S3}{R} \frac{V}{R} + \frac{S2}{2R} \frac{V}{2R} + \frac{S1}{4R} \frac{V}{4R} \right) \]

\[ = -\frac{R_f}{4R} V(4S3 + 2S2 + S1) \]
DA converter
DA pin signal
Connection of DAC

![Diagram of DAC connection]
Analog interfacing network
Analog-digital-analog path
Applications

• Body Sensor Network

• Personal Health Monitor
Body Sensor Network
Personal Health Monitor
Questions?